

Atty. Docket No. PIA30746/DBE/US
Serial No: 10/627,057

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Remarks

Applicant and his representatives wish to thank Examiner Wilczewski for the thorough examination of the present application and the detailed explanations in the Office Action dated February 27, 2007. The Examiner's concerns have been given serious consideration. However, the present claims are considered allowable over the cited references.

Claims 1-2 and 6-7 have been amended. Claims 11-14 were previously canceled. Claims 15-23 have been added. Thus, Claims 1-10 and 15-23 are active in the present application.

The present invention relates to a method for fabricating an RF semiconductor device comprising:

- a) forming a trench to define an active region and an element isolation region in a semiconductor substrate;
- b) forming a plurality of gate lines within the active region of the semiconductor substrate, the plurality of gate lines not extending over a center of the trench;
- c) forming an insulating layer on the plurality of gate lines and the semiconductor substrate;
- d) forming all contact holes in the insulating layer over the active region using a single pattern, wherein a first group of the contact holes exposes portions of the gate lines and a second group of the contact holes exposes portions of the substrate in the active region;
- e) forming contact plugs in each of the contact holes; and
- f) forming a conductive pattern layer over the insulating layer that is electrically connected with the contact plugs (see Claim 1 above).

The references cited against the claims fail to disclose or suggest forming a plurality of gate lines within an active region of a substrate, the plurality of gate lines not extending over a center of a trench; and forming all contact holes in an insulating layer over the active region using a single pattern, wherein a first group of the contact holes exposes portions of the gate lines

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and a second group of the contact holes exposes portions of the substrate in the active region (see, e.g., steps b and d above).

The Rejection of Claims 1-10 under 35 U.S.C. § 103(a)

The rejection of Claims 1-10 under 35 U.S.C. § 103(a) as being unpatentable over Park et al. (U.S. Pat. No. 6,511,919, hereinafter "Park") in view of Ishida (U.S. Pat. No. 6,642,555, hereinafter "Ishida") is respectfully traversed.

Claim 1 is exemplified by forming a plurality of gate lines 41 within an active region 30 of a semiconductor substrate 31, the plurality of gate lines 41 not extending over a center of a trench 13, forming an insulating layer 37 on the plurality of gate lines 41 and the semiconductor substrate 31, forming all contact holes 39 in the insulating layer 37 over the active region 30 using a single pattern, wherein a first group of the contact holes 39 exposes portions of the gate lines 41 and a second group of the contact holes 39 exposes portions of the substrate 31 in the active region 30 (see, e.g., paragraphs [0017]-[0021], and FIGS. 3-4b of the present specification).

The present invention reduces the overlap of the gate lines with an isolation region. For example, Claim 1 recites that the plurality of gate lines is formed within an active region, the plurality of gate lines not extending over a center of a trench. Since the gate lines 35 do not substantially overlap with isolation region trench 33, the parasitic capacitance between the gate lines 35 and the substrate 31 can be decreased, as well as the resistance of the gate lines 35, thereby improving the operating frequency of the device (see, e.g., paragraphs [0022]-[0023] of the specification; also compare FIGS. 1 and 3 of the present application).

Park discloses a method of forming a self-aligned contact holes in an oxide layer to expose a semiconductor substrate between adjacent gate lines (see, e.g., Abstract). More specifically, Park discloses that a nitride spacer 106 is formed between gate lines 104 and contacts 112 (see, e.g., col. 5, ll. 45-55, and FIG. 4D-4E). Contact holes 110 of Park do not expose the gate lines 104, which remain covered by nitride spacers 106 (see, e.g., 4D-4E). Thus,

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Park fails to disclose forming contact holes in an insulating layer over an active region, wherein a first group of the contact holes exposes portions of gate lines and a second group of the contact holes exposes portions of a substrate in the active region, as recited in Claim 1.

Furthermore, Park appears to disclose that some of the gate lines 104 run longitudinally over isolation structures 102 (see, e.g., FIGS. 4A-4E, and 5A-5B). Although Park does not affirmatively disclose that the gate lines extend over a center of the isolation structures 102, Figures 4A-4E and 5A-5B of Park show some of the gate lines 104 running longitudinally over the isolation structures 102. Thus, Park discloses that gate lines 104 substantially overlap with the isolation structures 102. Accordingly, Park neither discloses nor appreciates the benefits of the presently claimed method, which minimizes overlap of gate lines with isolation regions to thereby reduce parasitic capacitance and resistivity, as described above.

In view of the preceding discussion, Park is deficient with regard to the method of Claim 1.

Ishida discloses a semiconductor memory device having a plurality of memory cells wherein a substantial portion of gate line GL2 is formed over an isolation region 4 (see, e.g., FIGS. 5B, 6B, and 7B). As a result, Ishida discloses that gate line GL2 substantially overlaps with the isolation region 4. Thus, Ishida does not appear to disclose or appreciate the benefits of forming a plurality of gate lines within an active region of a semiconductor substrate, the plurality of gate lines not extending over a center of a trench, as recited in Claim 1.

In view of the preceding discussion, Ishida fails to cure the deficiencies of Park with regard to the method of Claim 1. Therefore, Claim 1 is patentable over Park in view of Ishida, and the rejection under 35 U.S.C. § 103(a) should be withdrawn.

Claims 2-10 depend from Claim 1, and therefore contain all of the limitations of Claim 1. Therefore, Claims 2-10 are patentable over Park in view of Ishida for essentially the same reasons as Claim 1.

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Conclusions

In view of the attached Declaration and above remarks, all bases for objection and rejection are overcome, and the application is in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,



Andrew D. Fortney, Ph.D.
Reg. No. 34,600

401 W. Fallbrook Ave., Suite 204
Fresno, California 93711
(559) 432 - 6847

ADF:wkn